APPLICATION NOTE

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

INTRODUCTION

The Model TBU-CA Series of Bourns® TBU® products are low capacitance single bidirectional high-speed protection components, constructed using MOSFET semiconductor technology, and designed to protect against faults caused by short circuits, AC power cross, induction and lightning surges. The TBU® high-speed protector placed in the system circuit will monitor the current with the MOSFET detection circuit triggering to provide an effective barrier behind which sensitive electronics will not be exposed to large voltages or currents during surge events.

PURPOSE

This application note analyzes the behavior of the Model TBU-CA during a surge event, while protecting an active line, and determines the time and conditions required to recover to the operating state (the state where the TBU® device is passive and not protecting).

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

SIMULATION

The test circuit in Figure 1 was simulated in order to understand the behavior of the TBU® device during a surge event. The circuit on the right side of Figure 1 represents an active signal, V_{SIGNAL}, (V3, R2, D1) into a load (R3) through an 850 V / 500 mA TBU® device (Bourns Part Number TBU-CA085-500-WH). The D1 diode is to help protect V3 from the 50 V surge.

Per the Model TBU-CA series data sheet, the series resistance of the Model TBU-CA085-500-WH is 10.7 Ω, typical. Also, the leakage current (I_Q) of the TBU® device while in protected state is 0.50 mA, typical.

The left side of Figure 1 represents a 50 V / 10 A surge controlled by a switch. For the sake of simulation, a voltage-controlled switch (S1) is controlled by a 5 V pulse (V2) that is 1 ms long (ramp up = ramp down = 5 ns).

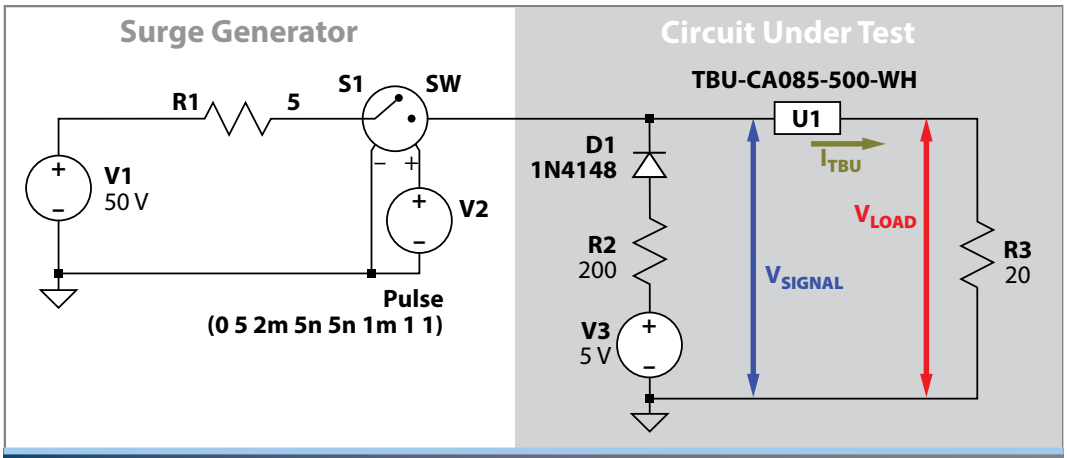

Figure 1 - Test Circuit

Model TBU-CA Series

SIMULATION (CONTINUED)

We can now compare the estimated values of V_{SIGNAL}, V_{LOAD}, and I_{TBU}, and measure the simulated values per the graph in Figure 2.

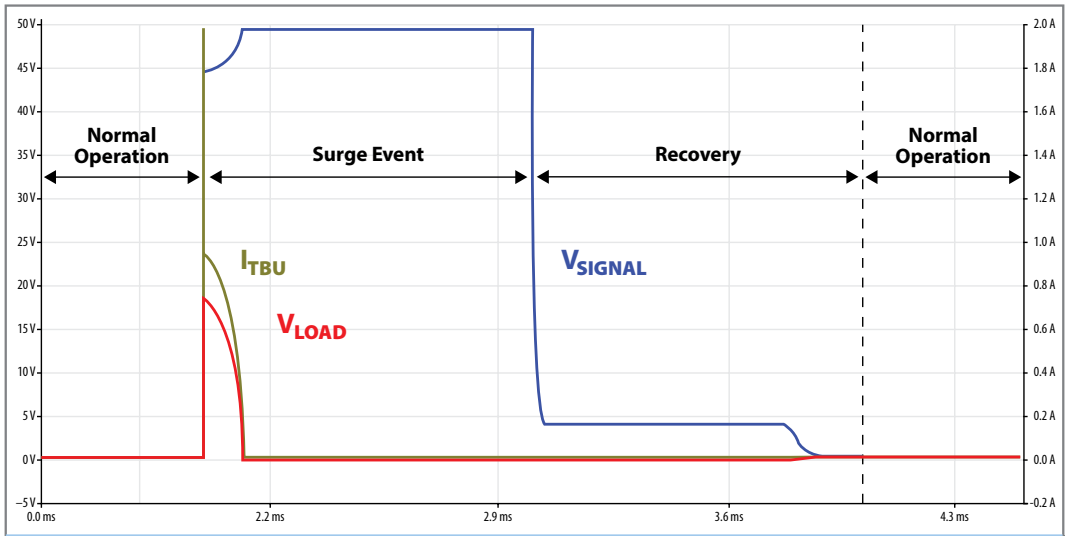

Figure 2 - Overall View of the Surge Event

During normal operation, assuming that the voltage drop across D1 = 0.7 V and the TBU® device's R_{DEVICE} = 10.7 Ω (both values will be different depending on SPICE models):

$$I_{TBU} = \frac{5 - 0.7\ V}{(200 + 10.7 + 20)\ \Omega} = 18.634\ mA$$

Per the simulation, I_{TBU} = 18.736 mA.

$$V_{SIGNAL} = 5\ V - (18.634\ mA \times 200\ \Omega) - 0.7\ V = 572.215\ mV$$

Per the simulation, V_{SIGNAL} is 525.171 mV.

$$V_{LOAD} = 0.572\ mV - (18.634mA \times 10.7\ \Omega) = 372.564\ mV$$

Per the simulation, V_{LOAD} is 374.722 mV.

During recovery, using the TBU® device's leakage current I_Q = 0.5 mA:

$$V_{SIGNAL} = 5\ V - (0.5\ mA \times 200\ \Omega) - 0.7\ V = 4.2\ V$$

Per the simulation, V_{SIGNAL} is 4.375 V.

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

SIMULATION (CONTINUED)

Looking at the surge current in Figure 3 – *Total time of the TBU® Device Going into Protected State (I_{TBU} decreasing to I_Q)*, the TBU® device's reaction time (current dropping I_Q) is about 120 µs. The time it takes for the TBU® device to start blocking is approximately 40 ns (Figure 4).

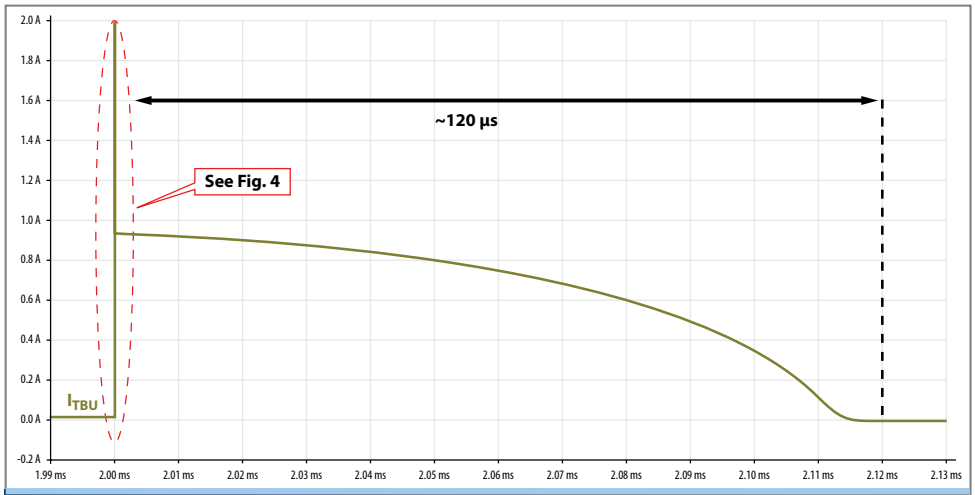

Figure 3 - Total Time of the TBU® Device Going into Protected State (I_{TBU} decreasing to I_Q)

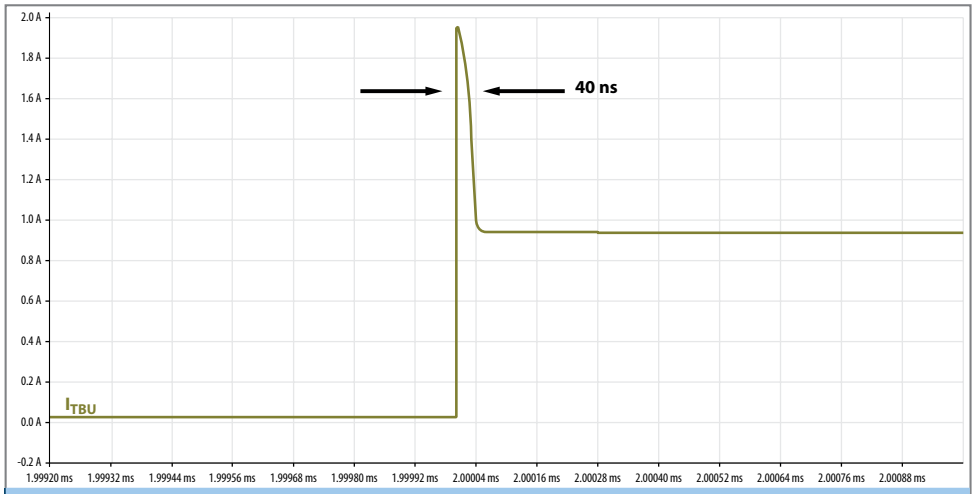

Figure 4 - Reaction Time of the TBU® Device to a surging I_{TBU}

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

SIMULATION (CONTINUED)

During recovery, the TBU® device is still in protected state. The TBU® device's leakage current (~0.5 mA) creates approximately 4.375 V at its input. The device stays in protected state for approximately 800 µs and ramps down for approximately 200 µs, back to normal operation. Per the simulation, we can approximate the total recovery time to be 1.0 ms ±15 %.

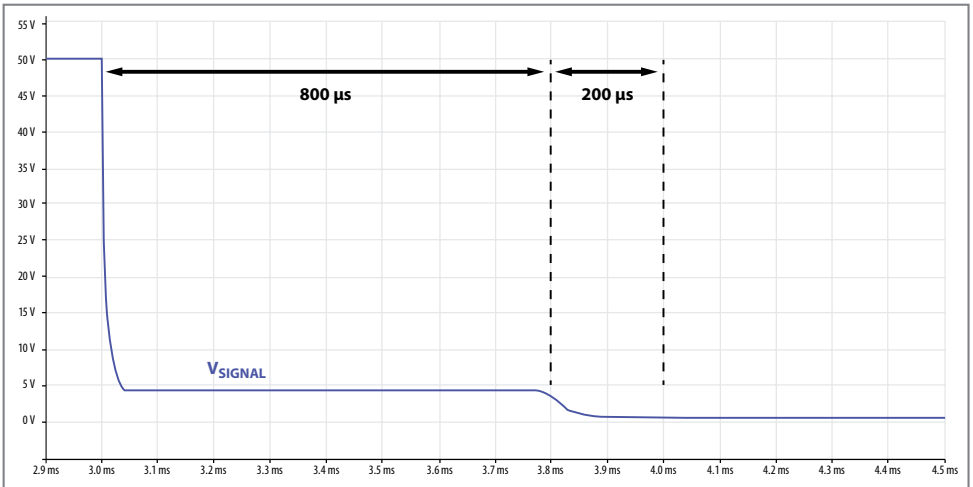

Figure 5 - Recovery at the Input of the TBU® Device

Model TBU-CA Series

SIMULATION (CONTINUED)

Next, we'll examine the TBU® device by looking at the voltage across it while varying the voltage source V3. This will help us understand the recovery times at different voltages, and how the device behaves as it approaches the reset voltage and above.

The simulated circuit is modified by stepping the V3 supply from 1 V to 20 V, 1 V at a time.

Per the data sheet, the Model TBU-CA reset voltage, V_{RESET}, is 12 V minimum. This is the voltage across the TBU® device.

As shown in Figure 6, the total recovery time for all signal levels is still within a microsecond of each other. But notice how at 17.40 V (when V3 = 18 V) the behavior starts to change and eventually, at higher voltages, the TBU® device does not reset.

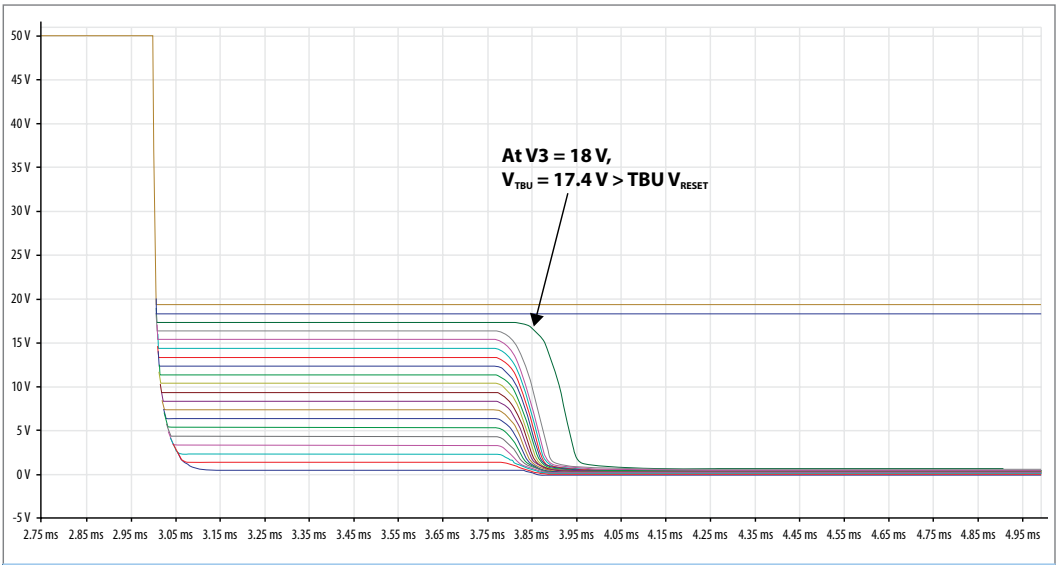

Figure 6 - Voltages Across the TBU® Device at Different Signal Levels, Simulation

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

BENCH TEST

The circuit was built to measure the actual behavior of the TBU® device. During normal operation, the surge event, and the recovery, we get the same behaviors as simulated, albeit a difference in timing (simulation vs. actual).

Starting at normal operation, Figure 7 demonstrates that V_{SIGNAL} and V_{LOAD} are very close to the estimated values, 575 mV and 375 mV, respectively.

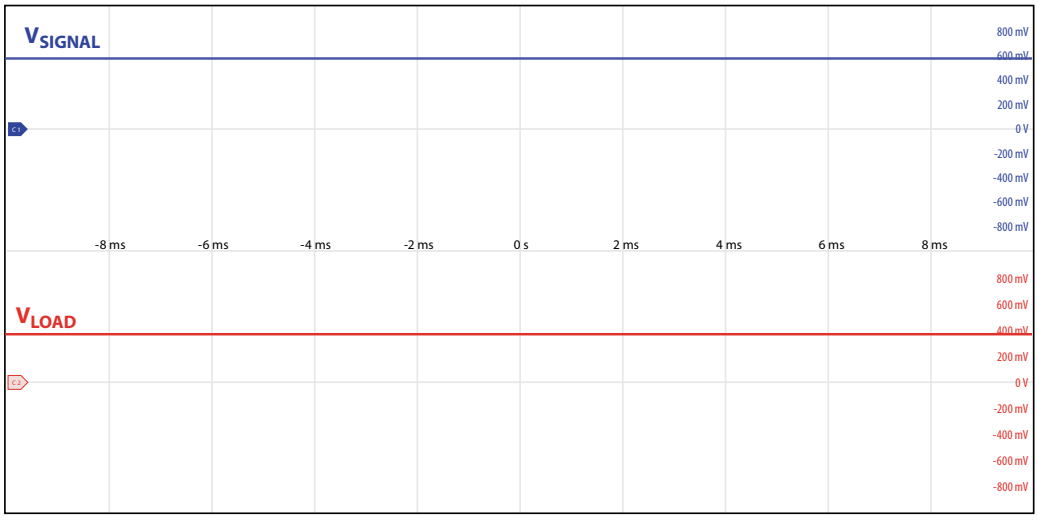

Figure 7 - Voltages at Normal Operation

Model TBU-CA Series

BENCH TEST (CONTINUED)

Here in Figure 8, we can see the effects of the TBU® device triggering. While the reaction time is under 2 µs, the TBU® device goes into protected state within 36 µs.

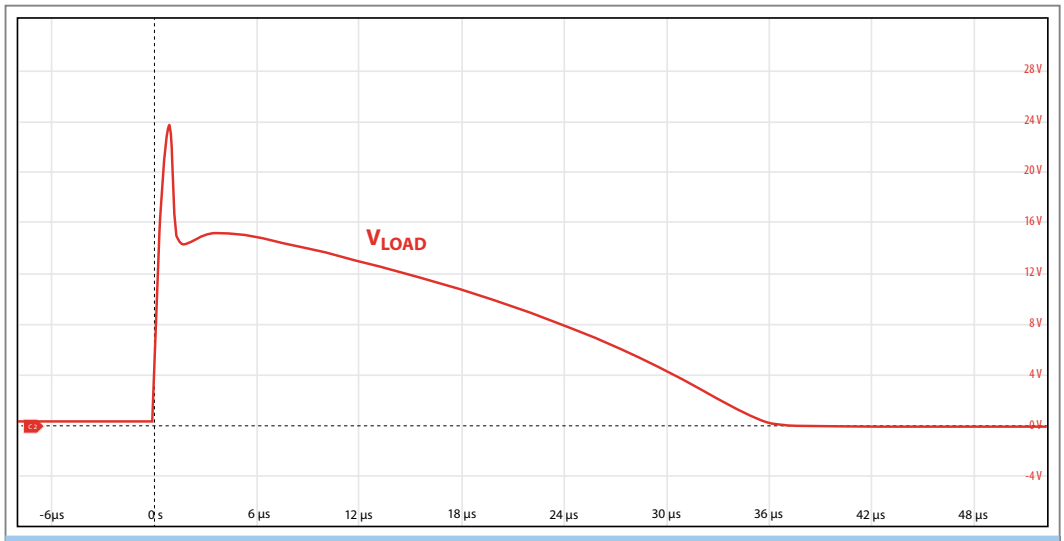

Figure 8 - Total Time of the TBU® Device Going Into Protected State

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

BENCH TEST (CONTINUED)

In Figure 9, V_{SIGNAL} at the input of the TBU® device shows the same behavior as the simulation during recovery. Here, the total recovery time is less than 250 µs. This time is much faster than the SPICE simulation.

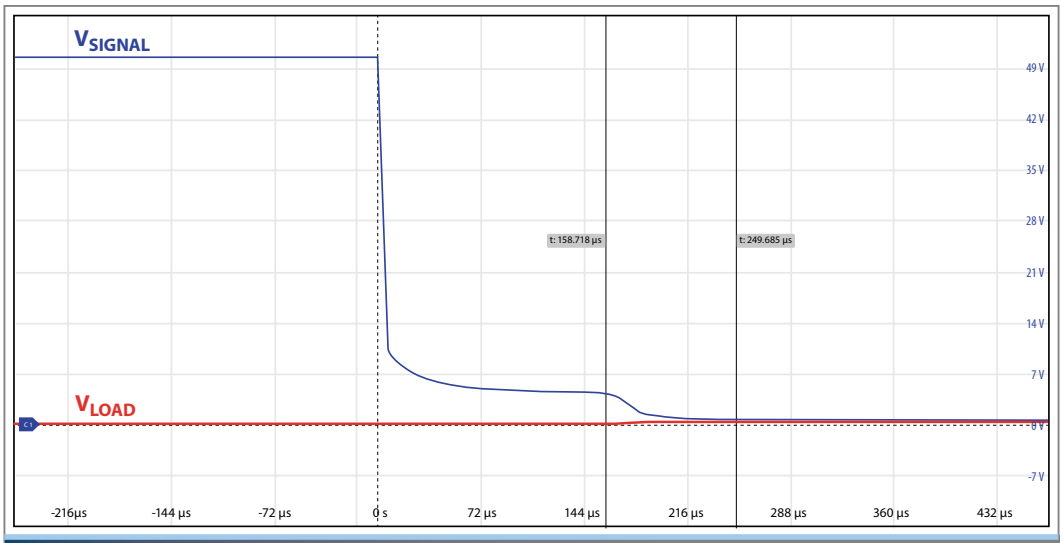

Figure 9 - TBU® Device Recovery at V_{SIGNAL}

Model TBU-CA Series

BENCH TEST (CONTINUED)

Figure 10 represents the behavior of the TBU® device at different signal voltage levels, during recovery time. Notice how, at V3 = 12 V, the TBU® device's behavior changes, and at V3 ≥ 15 V, the TBU® device does not recover (above the V_{RESET}).

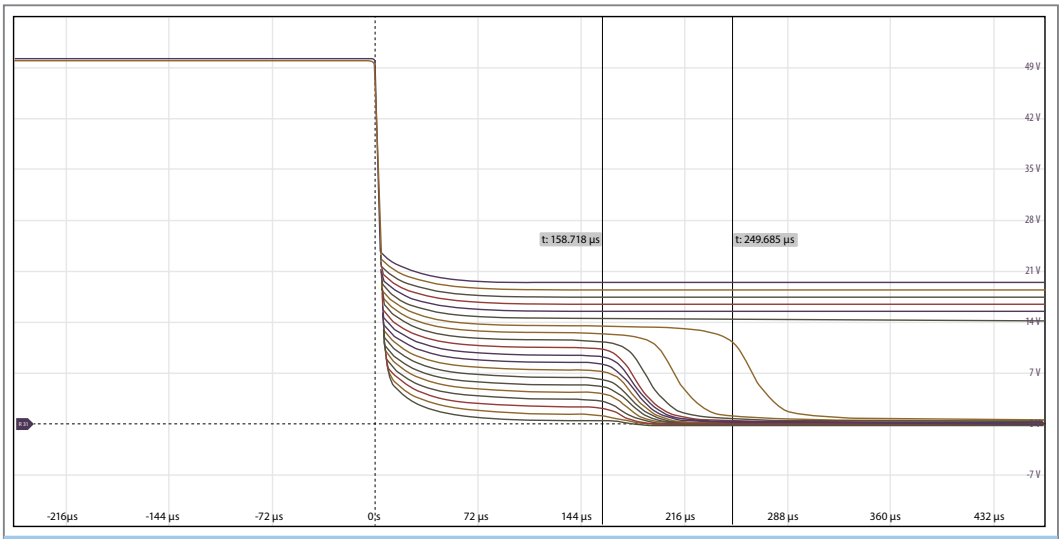

Figure 10 - Voltages Across the TBU® Device at Different Signal Levels, Actual

APPLICATION NOTE

Model TBU-CA Series - Modeling and Recovery Time Estimations

Model TBU-CA Series

SUMMARY

Based on the simulation bench testing, we've seen a difference in timing between both methods, although the behavior of the TBU® device SPICE model is still valid.

The TBU® device stays in a protected state approximately 160 µs after the surge event. The ramp-down (going from protected to safe operating state) takes an additional 70 µs to return to passive mode. The recommended time to allow the TBU® device to fully recover, while having a signal passing through, is approximately 250 µs.

The effects of the current through the TBU® device and/or the signal's voltage level is minimal, but it is observed that the recovery time is not certain when the TBU® device is operating closer to its reset voltage.

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