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APPLICATION NOTE

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Protecting High Speed Communication Ports

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USB Ports

The USB (Universal Serial Bus) specification provides a platform to allow a single USB port to drive 127 USB peripherals from a single host termination (PC). USB also allows remote powering from the host of a broad range of low power after-market accessories including travel lights, mobile phone chargers and laptop backup hard drives not requiring their own power supplies. USB 1.1 provided data transfer rates of up to 12 Mbps. The latest specification, USB 2.0, provides for data transfer rates up to 480 Mbps. USB 2.0 uses the standard A-plug that connects to the host and standard B-plug that fits into the peripheral. As these are too large for many portable units, mini A-plug and B-plugs are commonly used.

The latest USB OTG (On The Go) allows peripheral equipment (PDAs, digital cameras and mobile phones) to communicate with each other. For example, USB OTG allows digital cameras to send files directly to a printer without the use of a computer. Equipment with USB OTG has the ability to be either a host or a peripheral and can dynamically switch between the two. Equipment with USB OTG capability has smaller interface sockets. The connector can take either mini A-plugs or mini B-plugs and is called a mini-AB receptacle.

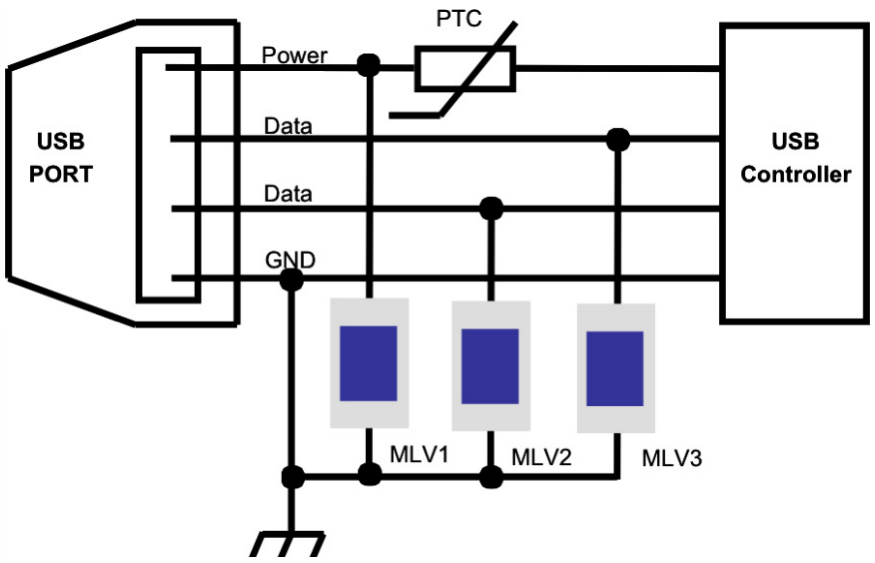

Figure 1

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IEEE 1394 (Firewire™, i.Link™) Ports

The IEEE published a serial bus standard called the IEEE 1394A that supports up to 400 Mbps and IEEE 1394B that supports higher data rates up to 800 Mbps. These standards also allow for isochronous data transfer that guarantees the bits per second rate. This is important in applications where streaming (real time) video is used or high volume data transfer is required. IEEE 1394 has also been designed to support up to sixty-three external devices from one port.

The IEEE 1394 layout is slightly different than USB in that two pairs of twisted pair cables are used for communication instead of one. The twisted pairs are individually shielded within the cable where one pair is used for data transmission and the other for data receiving. Cable screening is critical to reduce external interference that can cause data bit errors. The driver to receiver reversal is achieved through the cable. The ports are also terminated with a fixed resistor to provide accurate line termination (termination resistors are not shown in Figure 2).

A remote power feed option is also available that allows up to 45 W to be requested from the host. The power supply can support up to 1.5 A maximum with an absolute maximum voltage of 40 V. While this option does allow PDAs and digital cameras to be remotely powered, the high current density requires overcurrent protection to be present.

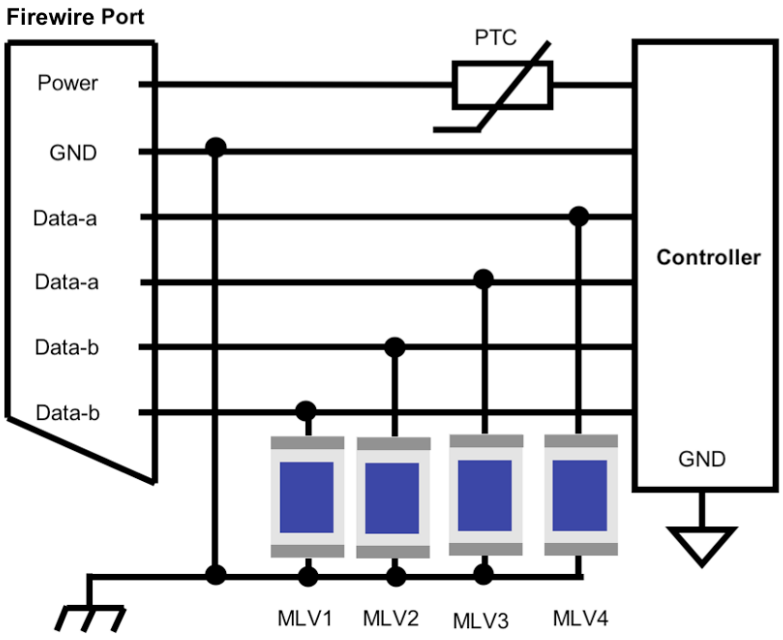

Figure 2

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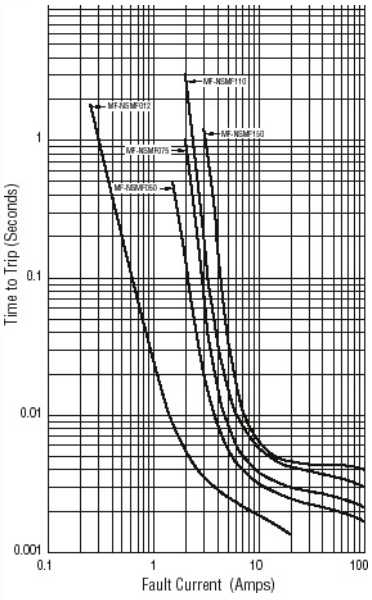
Overcurrent Protection for Power Lines

A positive temperature coefficient (PTC) thermistor's resistance significantly increases once the body temperature, through the heating effect (I^2R), is tripped. The trip resistance increases a few orders of magnitude higher than the original resistance. The hold current (I_{HOLD}) is the minimum current the PTC thermistor will conduct without tripping at the maximum voltage, Vmax. This parameter is usually specified at room temperature. An increase in ambient temperature results in a reduced trip current which should be considered in the design phase.

A PTC thermistor can go into its high resistance state anywhere between I_{HOLD} and I_{TRIP} and is largely dependent on the PTC thermistor's resistance. The PTC thermistor will stay in its tripped state with a low trip current until the current falls below its I_{HOLD} value. The holding current will be extremely low due to the elevated package temperature and therefore manual reset may be required. Once the PTC thermistor cools, the resistance returns to its nominal value. As the PTC thermistor trip is dependent upon current, there is a relationship between trip time and current. Low fault currents close to the trip current specification can exhibit long delay switch times which should also be considered in the design phase.

USB Overcurrent Protection for Power Lines

USB 2.0 host ports (desktop and laptop computers) can source up to 500 mA. External hubs are limited to 100 mA per port with a maximum of four ports per hub. The ports are nominal 5 V supplies where overcurrent protection is required. A USB OTG peripheral device is designed to act as a limited host and must be able to transmit and receive power. In such equipment, if the current rating per port is greater than 100 mA, then the voltage regulation is required to be between 4.75 V and 5.25 V. This ensures reverse compatibility with USB 2.0 specification requirements for power providers. USB 2.0 makes overcurrent protection a requirement and a polymer positive temperature coefficient (PPTC) thermistor can be considered. For example, the Bourns® Multifuse® MF-NSMF075 thermistor has an I_{HOLD} of 750 mA a 23 °C, but this drops to 520 mA at 60 °C. If a higher hold current is required, the MF-NSMF110 is specified at 800 mA at 60 °C to provide a small safety margin in the design. The trip current (I_{TRIP}) is twice the hold current and is the current at which the PTC thermistor will be in its tripped state.



For example, the MF-NSMF050 will take approximately 3 seconds to switch at 1 A load current with 0.15 seconds at 2 A. The lower resistance MF-NSMF075 will take approximately 1 second to trip under a 2 A load.

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The time-to-trip curve is also helpful to ensure that the PTC thermistor does not trip with high in-rush currents associated with power-on or hot plugging. The DC power supply also needs to support the short circuit current for the duration of the trip time.

The addition of a PTC thermistor will affect the load regulation of the USB supply. The supply load regulation should not drop below 4.75 V under maximum load conditions of the power supply. The maximum series resistance, including the DC power supply fictive resistance should be less than 0.5 Ω. The maximum USB cable resistance for five meters is 190 mΩ. The track resistance of 2 mΩ per centimeter can be considered with the resistance of the PTC thermistor, but this can typically be ignored. The PTC thermistor resistance may need to be reduced to ensure suitable regulation, but this will place more strain on the power supply under fault conditions.

Model	V_{MAX} Volts	I_{HOLD} mA	I_{HOLD} 60°C	I_{TRIP} mA	R_{MIN} Ohms	R_{MAX} Ohms
MF-NSMF050	13.2	0.50	0.35	1.00	0.15	0.70
MF-NSMF075	6.0	0.75	0.52	1.50	0.10	0.29
MF-NSMF110	**6.0**	**1.10**	**0.80**	**1.80**	**0.06**	**0.20**
MF-NSMF150	6.0	1.50	1.10	3.00	0.03	0.13

Figure 4

IEEE 1394 Overcurrent Protection for Power Lines

Most peripheral components today utilizing IEEE 1394 do not use remote powering features and some suppliers provide cable with the power lines removed. However, PDAs such as the iPod use this to their advantage when connected into the host. The IEEE 1394 specification has a higher power density compared to USB 2.0 and therefore the PTC thermistor consideration is a little different. The maximum voltage capability of the PTC thermistor needs to be at least 33 V with a trip current above 1.5 A. The Bourns® Multifuse® MF-SMDF150/33 thermistor has a hold current of 1.5 A at ambient temperatures to limit the short circuit current stress on the power supply. The MF-SMDF150/33 has a typical trip time of 120 seconds with a 2 A fault current and 7 seconds with 5 A to make it resistant to high in-rush current conditions. With a maximum package height of 1.09 mm and a 2018 footprint, it is suitable for use in smaller consumer applications.

Model	V_{MAX} Volts	I_{HOLD} mA	I_{HOLD} 60°C	I_{TRIP} mA	R_{MIN} Ohms	R_{MAX} Ohms
MF-SMDF150/33	**33**	**1.50**	**1.00**	**3.00**	**0.07**	**0.175**
MF-SM150/33	33	1.50	0.99	3.00	0.06	0.23
MF-SM185/33	33	1.8	1.28	3.60	0.04	0.15

Figure 5

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ESD Overvoltage Protection

The key to selecting overvoltage protection is to consider what the equipment needs to be protected *against.* Integrated circuits (ICs) are typically rated to 1-2 kV contact voltage to protect them against possible board manufacturing incidents. IEC 61000-4.2 specifies human body models up to 8 kV contact for ESD incursions that would be considered in portable equipment. IC protection with a Level 1 specification will become the secondary protection scheme where a primary protector is required against 8 kV impulses. The ESD protector has a reaction time associated with it when tested under the high dVdT (8 kV/ns) conditions that govern the overshoot of the protector. It is therefore important to ensure that the IC or circuit being protected can support this peak voltage. There are discussions to increase the contact and air discharge specifications since human body models can reach 25 kV in static-rich environments.

The most common method for ESD protection is to use small silicon based zener diodes or multilayer varistors (MLV) as the first level of protection against ESD. It is therefore important to know the power density that the protector needs to withstand to provide a reliable solution. The multilayer varistor has a threshold voltage where the initial resistance is high (120 MΩ for CG0603MLC family). As the voltage increases, the resistance reduces with a resultant exponential increase in the current through the device. This allows the overvoltage disturbance to be shunted away from the circuit it is protecting while the energy is dissipated in the protector. Once the electrical disturbance has passed, the MLV will return to its high resistance off state.

Overvoltage Protection for Data Lines

The capacitance of the protector becomes an issue for data lines where high baud rates are being designed. The series resistance with the load capacitance creates a first order filter that has the effect of slowing the rise and falling edge. Reducing the effective series resistance helps with wider track dimensions and copper weighting, but reducing the effective capacitance has the biggest impact. The Bourns® ChipGuard® CG0603MLC-xxE multilayer varistor was designed to provide ultra-low capacitance of 0.5 pF while having almost negligible leakage current. A 480 Mbps signal with the CG0603MLC device will have little effect on the data transfer rate and can be considered in 1 Gbps and higher type applications. For communication applications up to approximately 480 Mbps, the cost-effective CG0603MLD-xxE family with a higher maximum capacitance of 5 pF can be considered.

Overvoltage Protection for Power Lines

Power supplies are generally immune to ESD conditions due to the use of passive components such as capacitors and inductors that are inherently robust. Ferrite beads are commonly used to add additional series inductance to limit the impulse amplitudes under fast transients. This is usually sufficient protection, however, overvoltage protection solutions can also be considered to reduce the strain on the components. The 0603 type package can support a higher energy density than the 0402 and would be recommended for power line protection against ESD. The CG0603MLA-14KE has a maximum working voltage of 14 V, making it suitable for USB power line protection. To utilize one protector across the data and power ports, the CG0603MLD-12E or CG0603MLC-12E may be considered.

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IEEE 1394 applications require a higher standoff voltage to ensure the voltage is not clipped during normal operation. Bourns® ChipGuard® products do not currently support voltage options above 18 V and therefore the 400 W TVS (Transient Voltage Suppressor) CD214A-Txx zener diodes can be considered in these applications.

Layout Considerations

For transients to affect the power supply input/output of the USB controller, the transient must be in between the power line and system GND and therefore the varistor should be placed between the two connector terminals as close as possible to the external connector. Most portable equipment has only a system ground where the overvoltage protector will shunt the excess energy. This causes the whole system to be affected by the loop current and can cause ground bounce due to the inherent inductance in the PCB tracks.

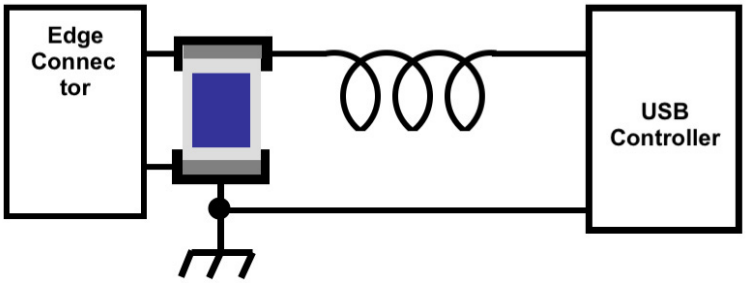

Figure 6

Inductive reactance is defined by the equation, $X_L = 2\pi FL$ where high frequency signals (ESD human body model equal to less than 1 ns rise time) will effectively increase the track resistance and therefore the voltage across it with the transient current. The inductance reactance can also be used as a benefit by further reducing ESD damage reaching critical components. The CG0603MLC-12E can have up to a 200 V absolute maximum peak impulse voltage, under ESD conditions. The impulse can be significantly reduced by placing the protector as far away from the IC (integrated circuit) as possible to provide additional series inductance between the two components as highlighted in Figure 6. The CG0603MLC-05E has a typical clamp voltage of 20 V (30 ns delay time to measurement) that is designed to lower overstress conditions. High voltages (6 kV or more) entering the board can cause flashover onto adjacent tracks and therefore, the overvoltage protector should be located as close as possible to the connector. The Bourns® ChipGuard® multilayer varistor should also be placed as close as possible to the communication lines where ideally the overvoltage protector pad should be integrated into the communication line. Having interconnects from the communication line to the protector introduces additional inductance. This track inductance becomes a hindrance as it is now in series with the varistor, which has the effect of increasing the initial overshoot of the device.
IC manufacturers discourage long track lengths between the connector and the IC as this can be deleterious to performance. Therefore, it is key to select a good quality ESD protector that has low overshoot and clamp voltage performance.

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Appendix

Electrostatic Discharge (ESD) is a charge that is exchanged between two objects of unequal charge potential. The most common event that ESD protects against is between people and metal objects. People with their movement can cause a build-up of electrons that behave like a capacitor if dielectric isolation is available. Manmade materials, such as a sole of a shoe, achieve dielectric isolation while a person is walking on carpet; this causes kinetic energy.

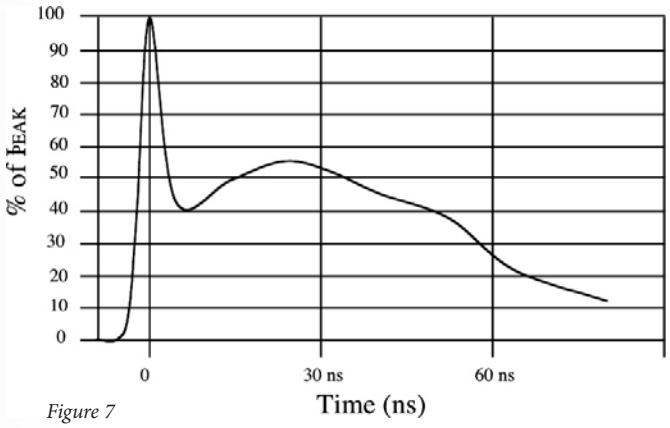

Figure 7

The International Electro-technical Commission (IEC) developed a human model ESD event that would allow designers to take adequate protection in their electrostatic applications. The IEC defined the ESD discharge impulse with a rise time of less than 1 ns and decay time of 60 ns as highlighted in Figure 7. The new standard was called the IEC 61000-4-2 where four levels were identified.

IC manufacturers of electrostatic sensitive devices design a level of protection into the IC to increase its robustness. However, these protection circuits can add cost to the design by consuming expensive silicon real estate. IC manufacturers design to standards to protect against board manufacturing processes such as IEC 61000-4-2 Level 1 to 2 kV contact voltage. Human body ESD voltages are nature-determined and can be 15 kV or more which will damage the IC. The IEC 61000-4-2 Level 4 is specified with an air discharge of up to 15 kV to take this into consideration. Therefore, it is common practice to protect all "people interactive" data ports to Level 4 to limit product damage and increase the robustness of the equipment. The external ESD protector then becomes the first level of protection with the IC providing residual second level protection in the design.

IEC61000-4-2 Level	Contact Voltage (kV)	Air Discharge Voltage (kV)	Peak Contact Current (A)	Contact Current @ 30 ns (A)	Contact Current @ 60 ns (A)
Level 1	2	2	7.5	4	2
Level 2	4	4	15	8	4
Level 3	6	8	22.5	12	6
Level 4	**8**	**15**	**30**	**16**	**8**

Figure 8

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